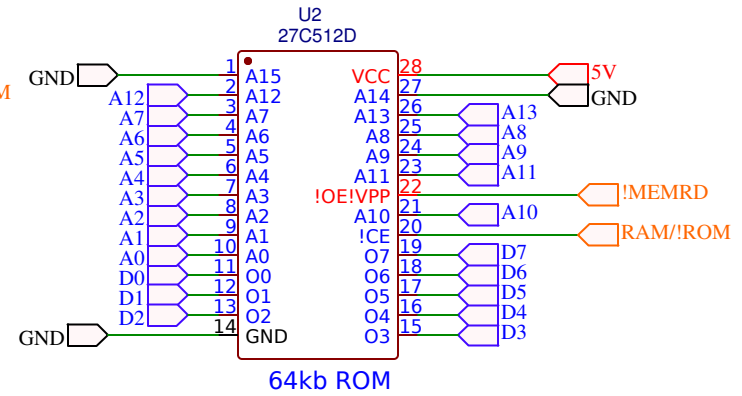
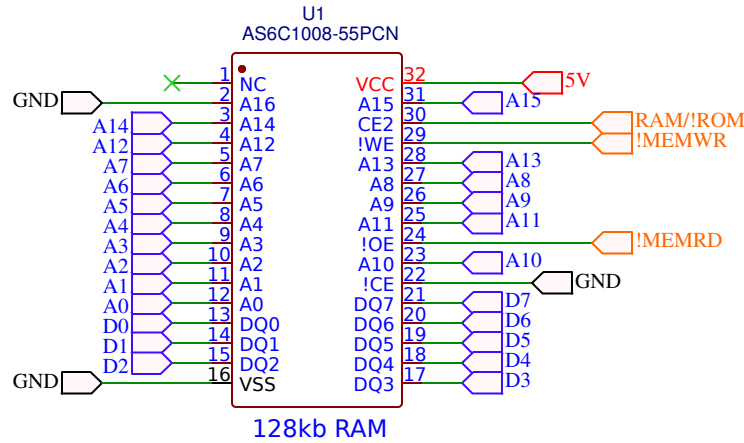
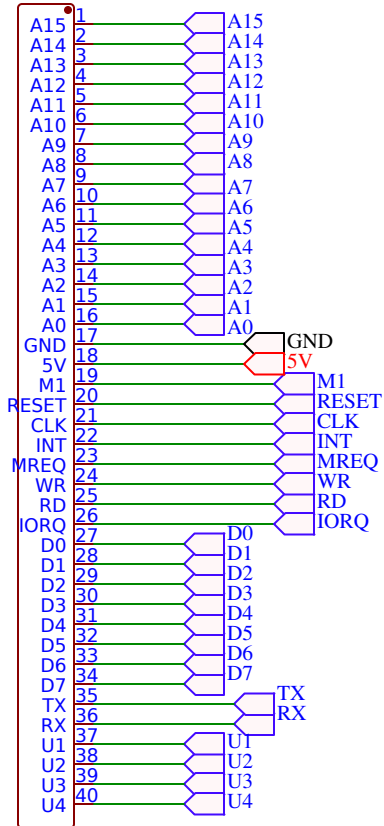
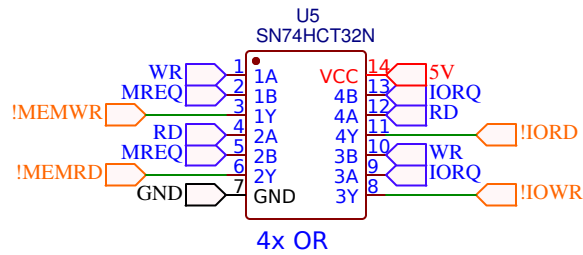


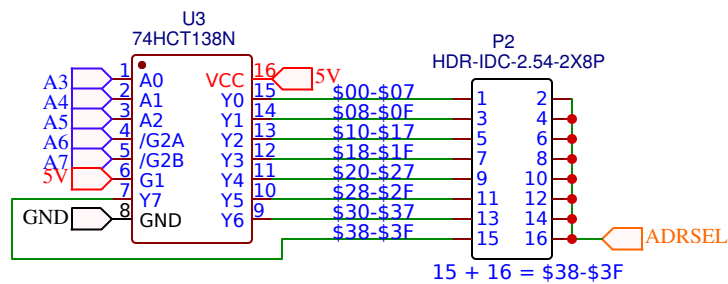
RC40_BUS
2.54mm 1x40P



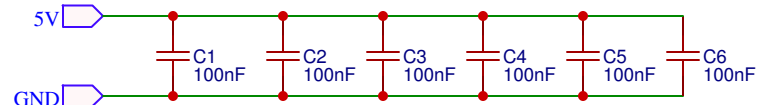
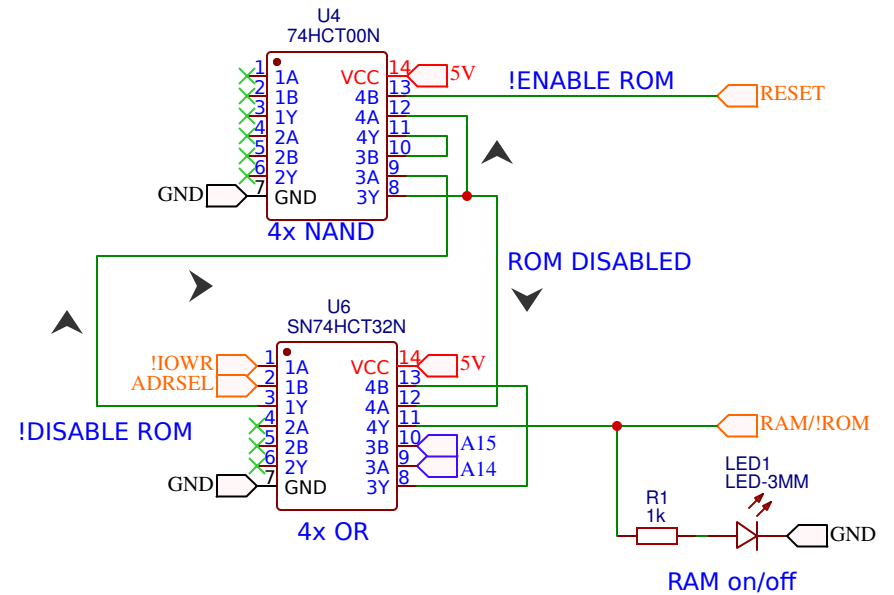
GENERATE BASIC SIGNALS



ADDRESS LOGIC



ROM SELECTION



| | | |
|------------------------------------|------------------|--------|
| TITLE: #45 Memory Module | | REV: C |
| Date: 2018-10-17 | Sheet: 1/1 | |
| EasyEDA V5.8.19 | Drawn By: karlab | |